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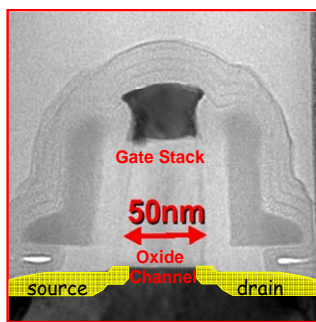
# Research Chairs

## Atomic-Scale Engineering for Si-Based Nanoelectronics

Co-funded by Applied Materials and Philips

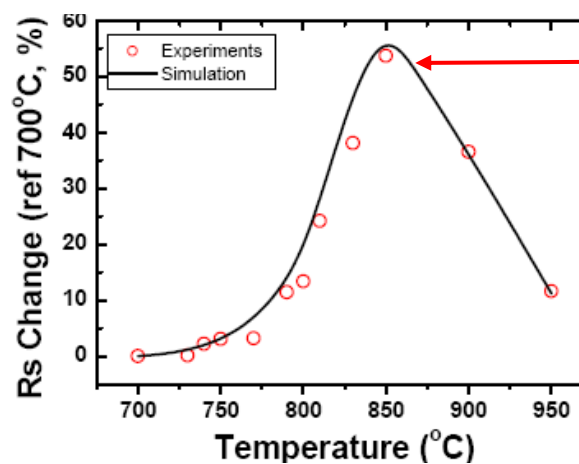
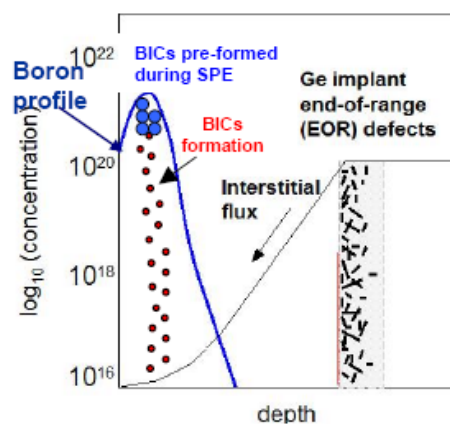
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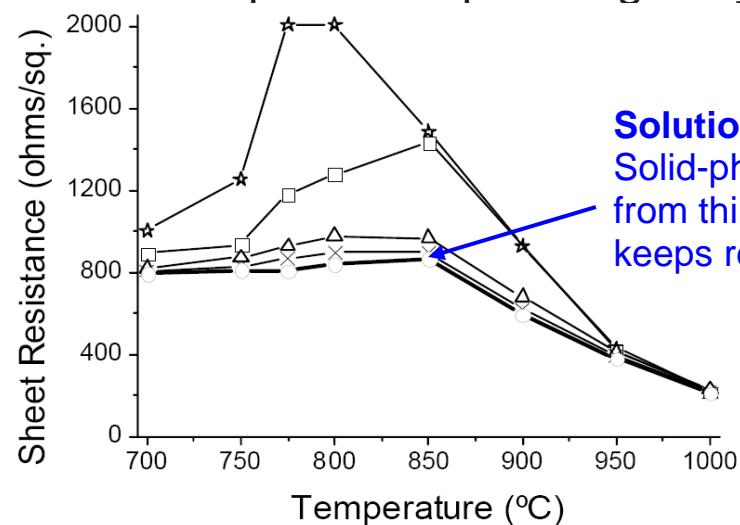
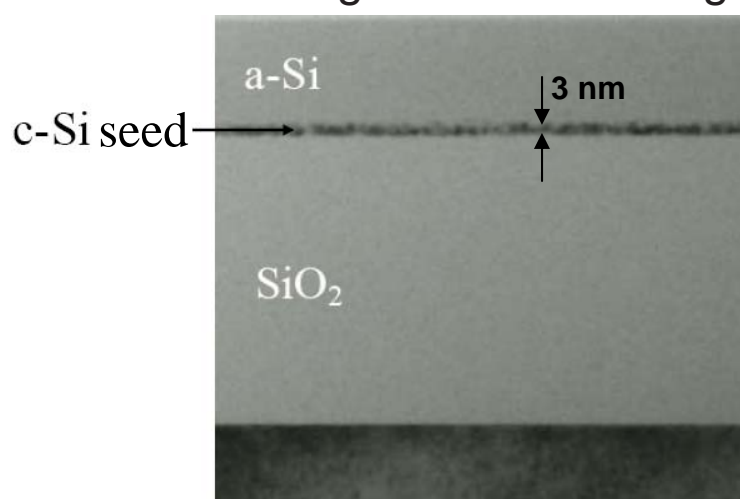
The performance of nanoscale silicon devices increasingly depends on mitigating the effects of atomic-sized defects, scarcely even visible by electron microscopy. Such defects are a key limitation for device performance. This work provides a 'toolkit' of solutions applicable to different device technologies - bulk, Silicon-on-Insulator, and non-planar devices like 'FinFets'.

One example is an approach we developed in collaboration with Applied Materials [1] and Philips [2]. A major technology issue arose from deactivation of dopant atoms in CMOS source and drain regions (figure above). Using a combination of experiments and computer modeling, we showed this was caused by the arrival of mobile 'interstitial' atoms evaporating from process-induced defects deep in the silicon.



**Problem**  
Large increase in sheet resistance during heat treatment, leading to device degradation

A range of solutions was found [3]. In one approach (for SOI technology) the defects are eliminated by rendering the active region amorphous, leaving only a thin crystal 'seed' that can grow on annealing to reconstruct a perfect doped single crystal.



**Solution**  
Solid-phase regrowth from thin crystal seed keeps resistance low

Ongoing work includes development of models for stress effects, diffusion and solubility in Si, SiGe and Ge, and self-organization in crystalline nanostructures.

[1] Applied Materials is an international semiconductor equipment company. In the UK it manufactures ion implanters, one of which was used in this work  
[2] Philips is an international electronics company. Its semiconductor division – the contact for this work – is now a separate company named NXP.  
[3] Presented at three IEEE International Electron Device Meetings – IEDM 2004 San Francisco (2 papers), IEDM 2005 Washington, and IEDM 2006.

